second isolation layer **62**, and the third shield sub-layer **53** is electrically isolated from the second shield sub-layer **52** by a third isolation layer **63**. In order to achieve an increase of the lateral breakdown voltage, the shield sub-layers **51**,**52**,**53** comprise end portions **71**,**72**,**73** respectively that extend over the drain extension region **7** and are essentially parallel to the top surface of the drain extension region **7**. The distance between the end portion **71** of the first shield sub-layer **51** and the drain extension region **7** is smaller than the distance between the end portion **72** of the second shield sub-layer **52** and the drain extension region **7**, and the distance between the end portion **72** of the second shield sub-layer **52** and the drain extension region **7** is smaller than the distance between the end portion **73** of the third shield sub-layer **53** and the drain extension region **7**. Furthermore, the end portion **73** of the third shield sub-layer **53** is further from the gate electrode **10** and closer to the drain contact region **6** than the end portion **72** of the second shield sub-layer **52**, and the end portion **72** of the second shield sub-layer **52** is further from the gate electrode **10** and closer to the drain contact region **6** than the end portion **71** of the first shield sub-layer **51**. This embodiment also achieves a similar improvement of the lateral breakdown voltage as the previously described embodiments.

[0033] FIG. **7** shows a cross-sectional view of another embodiment of the LDMOS transistor **1** according to the invention. In this embodiment the shield sub-layers **51**,**52**,**53** extend over the gate electrode **11** and at least partly over the source region **3** and the drain extension region **7**. Furthermore, the source region **3** and the substrate contact region **23** are mutually electrically connected with the first interconnect layer **24**. A contact to the first interconnect layer **24** may be made on a location which is outside the plane of the cross-section of FIG. **7**. This way of interconnecting the source region **3** and the substrate contact region **23** enables having a first shield layer contact **91**, a second shield layer contact **92** and a third shield layer contact **93** to electrically connect to the first shield sub-layer **51**, the second shield sub-layer **52** and the third shield sub-layer **53** respectively. The first, second and third shield sub-layer contacts **91**,**92**,**93** provide for a possibility to apply a voltage to the first, second and third shield sub-layers **51**,**52**,**53** respectively, thereby optimally influencing the distribution of the lateral electric field in the drain extension region **7** and further increasing the lateral breakdown voltage.

[0034] Optionally the first, second and third shield layer contacts **91**,**92**,**93** are electrically contacted to the first interconnect layer **24**, thereby reducing the amount of voltages that have to be applied to the LDMOS transistor **1**.

[0035] It should be noted that the shield layer **11** may also have other advantageous shapes, for example a combination with the stepped structure of the prior art WO 2005/022645 improves the current capability and the on-resistance of the LDMOS transistor **1**.

[0036] FIGS. **8**A-C show cross-sectional views illustrating a method for fabricating a MOS transistor according to an embodiment of the invention. FIG. **8**A shows a cross-sectional view of an LDMOS transistor **1** which has been fabricated, using conventional methods, up to and including the gate electrode **10** and which comprises, amongst others, the gate oxide layer **18**, the drain extension region **7** and the drain contact region **6**. Now, as is shown in FIG. **8**B, a staircase isolation region **121** is formed on a portion of the gate oxide layer **18** that extends over the drain extension region **7** by conventional deposition, photolithographic and etching techniques. The staircase isolation region **121** comprises a first isolation region **121*a*** and a second isolation region **122*b*** having a thickness larger than a thickness of the first isolation region **121*a***. The adjoining first and second isolation regions **121*a***, **121*b*** comprise an electrically isolating material, such as for example silicon dioxide. Thereafter, as is illustrated in FIG. **8**C, an isolation layer **14** is deposited and a shield layer **11** is formed extending over the first isolation region **121*a*** and at least over a part of the second isolation region **121*b***. The staircase isolation region **121**, comprising the first and the second isolation regions **121*a***, **121*b***, provides for a distance between the shield layer **11** and the drain extension region **7** which increases in a direction from the gate electrode **10** towards the drain contact region **6**. It should be noted that the staircase isolation region **121** may comprise additional isolation regions with an increasing thickness.

[0037] The staircase isolation region **121** may also be fabricated in an earlier phase of the process, for example just before the formation of the gate oxide layer **18**. Standard photolithographic, oxide growth and etching techniques may be applied to form a staircase isolation region **121** that extends over the drain extension region **7**.

[0038] Alternatively, as is shown in FIG. **9**, an inclining isolation region **131** may be fabricated which thickness increases in a direction away from the gate electrode **10** by applying well-known etching methods which provide for a tapered sidewall **132**. The slope of the tapered sidewall **132** depends, amongst others, on the resist and polymers that cover the sidewall **132** during etching and on the subsequent furnace curing parameters, such as temperature and time.

[0039] In summary, the MOS transistor of the invention comprises a gate electrode, a channel region, a drain contact region and a drain extension region mutually connecting the channel region and the drain contact region. The MOS transistor further comprises a shield layer which extends over the drain extension region wherein the distance between the shield layer and the drain extension region increases in a direction from the gate electrode towards the drain contact region. In this way the lateral breakdown voltage of the MOS transistor is increased to a level at which the MOS transistor may fulfill the ruggedness requirement for broadcast applications for a supply voltage higher than that used in base station applications.

[0040] It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of other elements or steps than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements.

1. A MOS transistor comprising a semiconductor substrate region in which a source region, a channel region, a drain extension region and a drain contact region are provided, wherein the drain extension region mutually connects the drain contact region and the channel region, and wherein the channel region mutually connects the drain extension region and the source region, the MOS transistor further comprising a gate electrode, extending over the channel region, and a shield layer of an electrically conductive material extending at least over a part of the drain extension region, wherein a